Remarks

Claims 1-22 are pending in the application.

Claims 1-22 are rejected by the Examiner.

Claims 1-4, 6, 8, 10-11, 14-18, and 20-21 are rejected under 35 USC 102(e) as being anticipated by Kagan et al. (US 6,243,787).

Claims 5, 7, 9, 12-13, 19 and 22 are rejected under 35 USC 103(a) as being unpatentable over Kagan et al. in view of Dobson et al. (US 6,766,386).

Claims 1, 8, 14, and 18 are amended.

Claims 1-22 remain in the case for consideration.

No new subject matter is added.

Reconsideration and allowance of claims 1-22 is requested in light of the above amendments and the following remarks.

Claim Rejections – 35 USC § 102

The Examiner rejects claims 1-4, 6, 8, 10-11, 14-18, and 20-21 as being anticipated over Kagan. The Applicant traverses the Examiner's rejections for the reasons that follow.

Claim 1 has been amended to recite *generate an indicator of completion to the system processor to indicate the completion of the data transmission to the system processor.* See Specification, page 6, lines 1-2.

The Examiner alleges that Kagan discloses this limitation, citing Col. 6, lines 33-44. But Kagan does not teach an indicator of completion to the system processor to indicate the completion of the data transmission to the system processor.

First, the Examiner is mistaken equating the interrupt cause as the indicator of completion recited in claim 1. The interrupt cause is not an indicator of completion to the system processor

to indicate the completion of the data transmission to the system processor, but rather it is an instruction to CPU 21 to read data from memory 22. See Col. 6, lines 36-39. If one attempts to equate the interrupt cause with the indicator of completion to indicate the completion of the data transmission to the system processor, further discussion in Kagan counters this argument. Because Kagan specifically requires a delivery completion step 74 as shown in FIG. 3, separately and independently from the interrupt cause, to ensure that all of the data have been written to memory 22 before CPU 21 can service the interrupt. See Col. 7, lines 26-29.

More importantly, Kagan does not generate an indicator of completion to the system processor to indicate the completion of the data transmission to the system processor. Instead Kagan teaches that the system memory or system controller generates an acknowledgment to the interface units (e.g., 40, 28) to acknowledged that all of the data is received in the system memory or system controller. For example, Kagan describes that the controller 46 of target interface unit 40 is programmed to send the interrupt packet only after receiving the acknowledgment from memory 22. See Col. 7, lines 29-32. In addition, Kagan describes that the controller 36 waits to assert the interrupt until the system controller 24 has acknowledged to HCA 32 that it has received all of the data. See Col. 7, lines 33-35.

If the acknowledgment is considered as an equivalent of the indicator of completion, then instead of generating an indicator of completion to the system processor, Kagan generates an indicator of completion from the system process to the interface units (e.g., interface units 44 and 28).

Claim 1 has also been amended to recite *insert the indicator into the transaction queue in the data path to a system memory associated with the system processor after the set of data*. See Specification, page 6, lines 10-11.

As discussed above, Kagan does not teach generating an indicator of completion to the system processor to indicate the completion of the data transmission to the system processor; logically Kagan cannot teach inserting such an indicator of completion into the transaction queue in a data path to a system memory associated with the system processor.

The Examiner alleges that Kagan teaches this limitation, citing Col. 7, lines 44-56. But the only relevant sentence in that paragraph states "the interrupt packet reached HCA32 after the last of the data packets (which will be the case when all of the packets are sent over the same channel, as described above)...." See Col. 7, lines 44-47. In other words, the interrupt packet is sent over the same channel as the data packets addressed to HCA 32 after the last of the data packets are sent. See Col. 6, lines 49-51, lines 48-49, and lines 23-25.

First, as discussed above, the interrupt packet is not the indicator of completion as recited in claim 1. Even if it is, the interrupt packet is inserted into the transaction queue in the same path addressed to HCA 32 after the set of data, not to a system memory associated with the system processor as in claim 1.

Claim 8, 14, and 18 recite identical limitations as in claim 1, but in a different format. Kagan does not teach all of the limitations recited in the independent claims 1, 8, 14, and 18, much less in the embodiments of their respective dependent claims. Claims 1-4, 6, 8, 10-11, 14-18, and 20-21 are patentably distinguishable from prior art and allowance is requested.

Claim Rejections – 35 USC § 103

The Examiner rejects claims 5, 7, 9, 12-13, 19 and 22 for obviousness over Kagan in view of Dobson. The Applicant traverses the Examiner's rejections for the reasons that follow.

Even though the Examiner may have suggested that Dobson discloses the limitations as in claims 5, 7, 9, 12-13, 19 and 22, the addition of Dobson to the combination does not overcome

the deficiencies of Kagan for the reasons discussed above. Therefore claims 5, 7, 9, 12-13, 19 and 22 are patentably distinguishable over the prior art and allowance of these claims is requested.

No new matter has been added by this amendment. Allowance of all claims is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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